A New Piezoelectric Transformer Driving Topology for Universal Input AC/DC Adapter using a Constant Frequency PWM Control

Myounghwan Ryu, Sungjin Choi, Sangmin Lee and Bo H. Cho

Seoul National University
School of Electrical Engineering and Computer Science
#043 San 56-1 Shilim-dong Gwanak-gu
Seoul, Korea.
Phone : +82-2-880-1785, Fax : +82-2-878-1452
Email : nanta97@pesl.snu.ac.kr

Abstract -- Generally, a Piezoelectric Transformer (PT) converter with frequency control has the characteristic which decreases the efficiency of PT in the wide input range. To improve this drawback, this paper introduces a constant frequency PWM control inverter topology for the PT which provides ZVS condition nearly independent of the load and line variation, and line regulation for the universal input as well. The main idea of the proposed PT converter is a buck-boost type driver utilizing the active-clamp circuit, and its output voltage is regulated by controlling the input voltage of PT primary side at the fixed switching frequency. The operation of the proposed converter is analyzed and the performance of the converter is verified by a 40[W] hardware prototype.

I. INTRODUCTION

The Piezoelectric Transformer (PT) may be a viable alternative to the magnetic transformer in some applications because the PT provides certain advantage over the magnetic transformer. One of the advantages is that PTs operate without the electromagnetic interface (EMI) because PTs are not based on the magnetic energy transfer. The PTs can also provide high voltage stepping ratio and does not require copper windings therefore it imposes saving in copper usage especially for large voltage conversion difference [1-5].

This paper presents a miniaturized AC adapter using the PT. The schematic diagram of a PT adapter is shown in Fig. 1. To drive a PT, an inverter switching frequency is determined by the PT's mechanical resonant frequency.

In the design of a PT adapter, there are two control methods. One is the pulse frequency modulation (PFM) control method and the other is the pulse width modulation (PWM) control method. It is known that the maximum PT efficiency can be obtained when it operates near the resonant frequency of the PT. As the operating frequency moves away from the resonant frequency, the PT efficiency decreases due to the increase of the circulating current [6-12]. Thus an AC/DC PT adapter using PFM control method for a wide input voltage variation reveals a poor efficiency and thermal problem especially at the high line condition.

This work is supported by Ministry of Commerce, Industry and Economy (MOCIE) and Piezo Solution Technology (PST) Co. Ltd, in Korea.

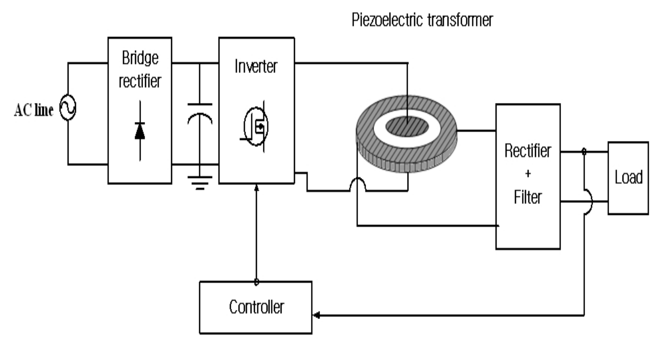


Fig.1. A schematic diagram of typical PT converter

Hence, it is necessary to fix the operating frequency near the resonant frequency of a PT under the variable conditions (load and input voltage variation, temperature changes, etc.) [2]. Thus, a PT converter using PWM control method has been suggested to overcome this problem [9]. However, the converter topology in [9] has a limited control range due to its step-up function and a combination of PFM control suggested in [10].

In this paper, a topology is introduced for the PT adapter which uses a constant frequency PWM control method providing ZVS condition almost independent of load and line variation with step down and step up features.

II. THE PROPOSED PT ADAPTER

Figure 2 shows the proposed circuit configuration of the PT converter with an active-clamp circuit. Switches S1 and S2 are turned on and off alternately with a short dead time. During the dead time, the energy stored in L_p, charges and discharges the output capacitors of the switches and the input capacitor, C_{d1}, of the PT. As a result, the ZVS operation is nearly independent on the load and input voltage variations. The amplitude of voltage, V_1, depends on the duty ratio of the main switch. Thus, output voltage, V_2 can be controlled by the duty ratio with a fixed frequency at which the PT efficiency is maximized.

A. Operational mode analysis

The mode of operations is illustrated in Fig's.3 and 4. In this topology, the capacitor, C_r, is sufficiently large to supply a constant voltage to the PT primary side.

Mode 1[t_1-t_2] : S1 turns on. The PT primary side voltage equals V_{IN} and the parallel inductor current i_{Lp} increases linearly.

Mode 2[t_2-t_3] : S1 turns off. The parallel inductor current, i_{Lp} charges the output capacitor of S1 and discharges the output capacitor of S2 to zero.

Mode 3[t_3-t_4] : Under the zero voltage condition, the low-side switch, S2, turns on, the parallel inductor current i_{Lp} decreases lineally and the voltage of capacitor, V_{Cr}. is supplied to the PT primary side and the voltage second balance of the parallel inductor is also achieved. The capacitor voltage is given by Eq.(4).

$$V_{Cr} = \frac{D}{1-D} V_{in} \tag{4}$$

Mode 4[t_4-t_5] : S2 turns off. The parallel inductor current discharges the output capacitor of S1 and V_1 becomes V_{IN}.

To achieve ZVS of the switches, the energy stored in the parallel inductance must be greater than the energy required to discharge the output capacitor during the dead-time, T_d.

$$\begin{aligned} C_T &= C_{ds1} + C_{ds2} + C_{d1} \\ \frac{1}{2} L_P I_{Lp}{}^2 &\geq \frac{1}{2} C_T V_{ds}{}^2 \end{aligned} \tag{5}$$

The value, I_{Lp} in Eq.(5) is almost independent of the load and also remains constant for the line variation. Thus, ZVS condition is independent of the load and line variation.

B. Fundamental gain approximation

Since the operating frequency is set near the resonant frequency of the band-pass filter characteristic of the PT, a fundamental approximation is used to derive the gain of inverter as a function of duty ratio. The fundamental amplitude of the PT primary voltage, V_1, is given by Eq.(6) and the conventional one in [9] is given by Eq.(7)

The proposed PT inverter stage:

$$V_1 = V_{in} \frac{2}{\pi \cdot (1-D)} \sin(\pi D) \tag{6}$$

The conventional PT inverter stage:

$$V_1 = V_{in} \frac{2 \cdot (2-D)}{\pi \cdot (1-D)} \sin(\pi D) \tag{7}$$

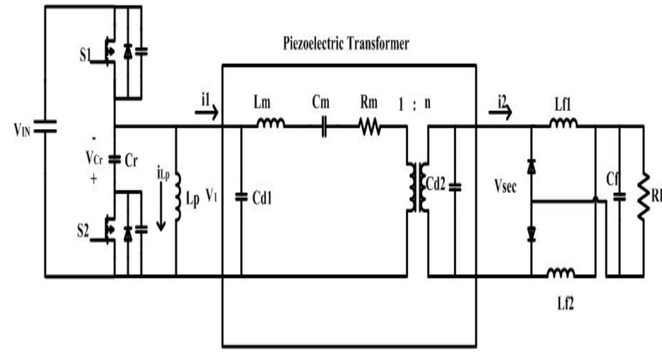


Fig.2. The proposed PT converter using PWM control

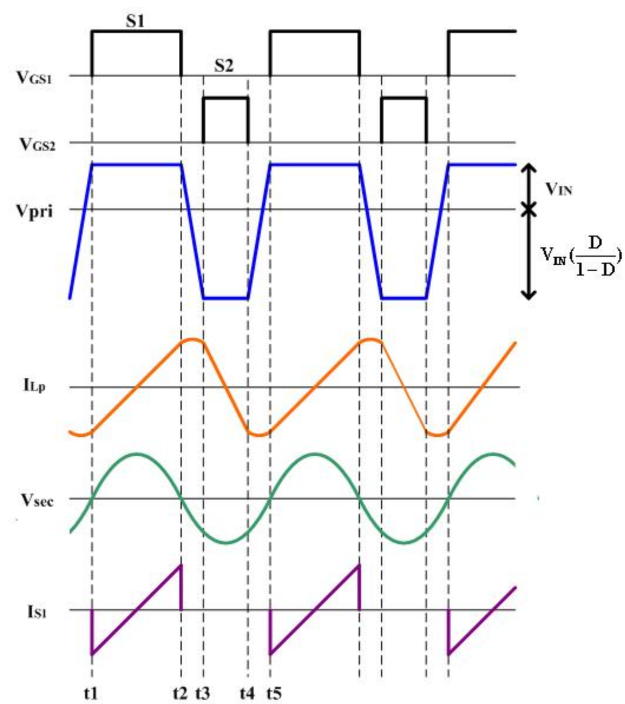


Fig.3. Key waveform of PT converter

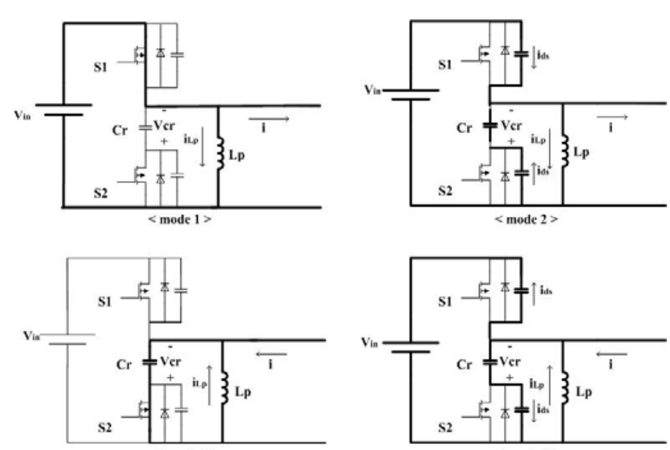


Fig.4. Operating mode of PT driving circuit

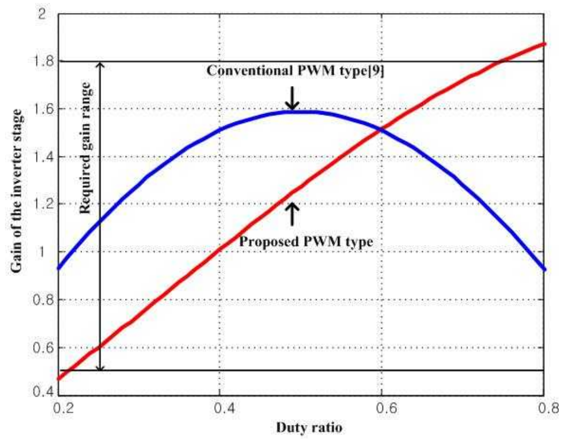


Fig.5. Controllability of duty ratio

Due to the ZVS condition and PT efficiency, sufficient deadtime is needed and the control range of duty is limited at 0.2 to 0.8. Therefore, in the universal input application, it is necessary for the PT converter to have wide gain range of 0.5-1.8 at the inverter stage for PWM control within the limit of duty ratio. Fig.5 shows that the proposed circuit can cover wider voltage gain range, which is required in a universal input but the conventional PWM PT converter has a limited gain range.

C. Current-Doubler Rectifier

The generated charges on the output electrode caused by the mechanical vibrations of the PT perform as a sinusoidal voltage source. The voltage, V_2, is an output of the PT and to calculate the voltage conversion ratio of the PT, the relation between V_2 and V_O must be derived. Accordingly, the derivation method of the ac resistance R_{eq} and the relation between V_2 and V_O are explained in [11-12].

$$V_o = \frac{1}{\pi} V_2 - V_F \qquad (8)$$

$$R_{eq} = \frac{\pi^2}{2} R_L \qquad (9)$$

where, V_F is the forward voltage drop of a rectifying diode, V_O is the output dc voltage, and R_L is the load resistance.

III. Experimental Result

The circuit and PT parameter values of the prototype are shown in table I. Fig.6 shows the PT driving waveforms. It can be observed from the inductor voltage that the switch operates with ZVS successfully.

The design specifications are as follows:

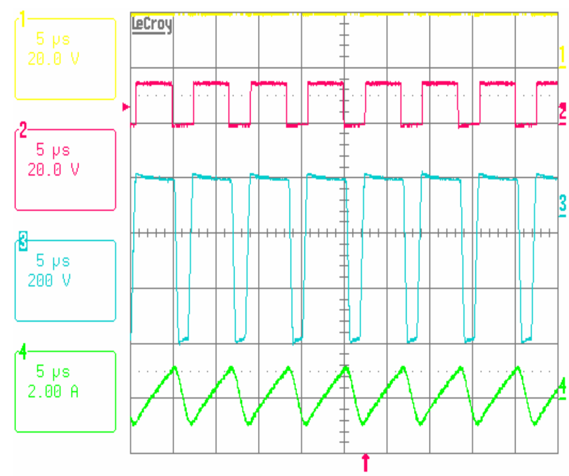
- Input voltage : 100 ~ 250[V_{rms}]
- Output voltage : DC 20[V]
- Output load : 1.5 ~ 2[A] (R_L=10~13[Ω])
- Operating frequency : 149 [KHz]

The H/W prototype consists of:

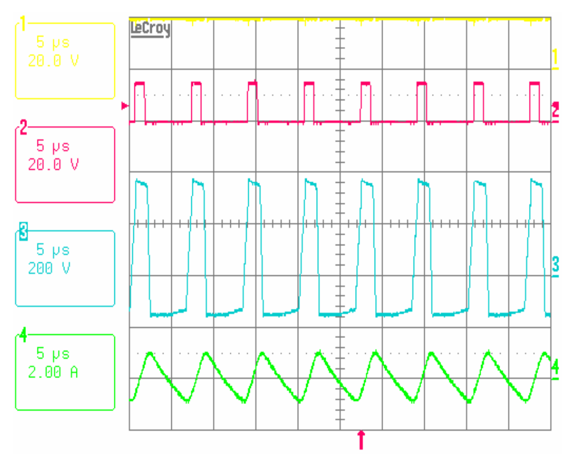
- Bulk capacitor: 400V 4.7uF Electrolytic. (Rubicon)
- Mosfet : FQP5N80
  (800[V]/5[A] DPAK Coss : 95[pF], Fairchild)
- Piezo Transformer: PZT #40A-17 (Dong-il Tech.)
- Controller: TL494

Table I. Circuit and PT parameter values of the prototype

parameter	Value	PT	Value	PT	Value
Cr	630V/ 330nF	L_m	15mH	C_{d1}	829pF
Lp	300uH	C_m	79pF	C_{d2}	20nF
Lf / Cf	500uH / 220uF	R_m	51 Ω	N	0.19



(a) V_{ac} = 100[V]



(b) V_{ac} = 250[V]

Fig.6. Hardware waveforms (ch1: output voltage, ch2: high side gate signal, ch3: PT primary voltage (V_1), ch4: inductor current (i_{Lp}))

Figure 7 shows the duty ratio range vs. input voltage. Fig.8 shows the efficiency of the PT for the duty ratio and frequency variation. From this figures, it is verified that for the efficiency of PT, frequency variation is more sensitive than harmonics of driving waveform.

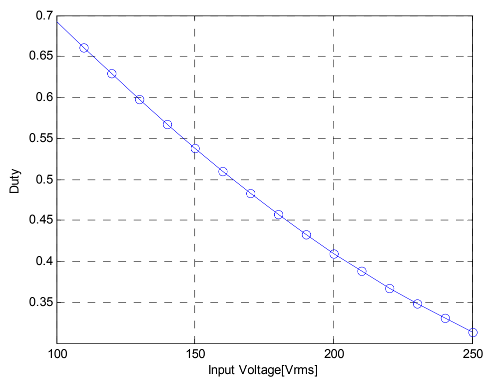


Fig.7. Input voltages vs. Duty ratio

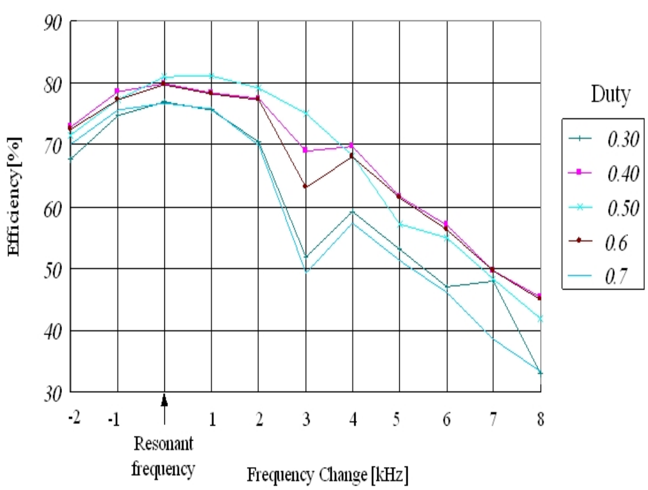


Fig.8. Measured efficiency of PT

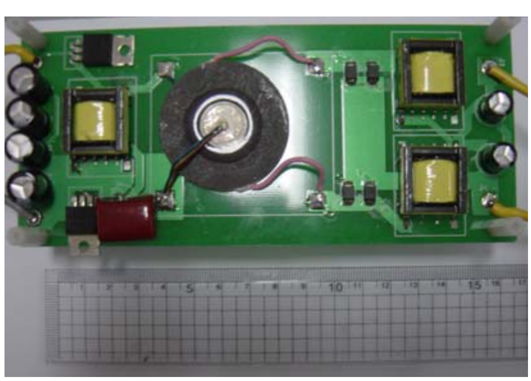


Fig.9. Hardware Prototype

IV. CONCLUSION

In this paper, an improved PT adapter topology for universal input is proposed. The proposed topology provides the ZVS operation for both of the main switch pairs in the load and input voltage variations. It is shown that a constant frequency with PWM control offers higher efficiency than PFM control. The proposed topology, which has a step up/down function, is more adaptable for the universal input application providing a wider gain range than the conventional one. Its operation and performance were verified by a 40[W] hardware prototype.

REFERENCES

[1] K.F. Kwok, P. Dong, K.W.E. Cheng, Kwok K.W, Y.L. Ho, X.X. Wang and H. Chan, " General study on piezoelectric transformer," Power Electronics Systems and Applications, 2004, Nov. 2004, pp. 216 – 220.

[2] G. Ivensky, I. Zafrany and S. Ben-Yaakov, "Generic operational characteristics of piezoelectric transformers," PESC '00. June 2000, pp. 1657 – 1662.

[3] S. Ben-Yaakov and S. Lineykin, "Frequency tracking to maximum power of piezoelectric transformer HV converters under load variations," PESC '02, June 2002, pp. 657 – 662.

[4] R. Prieto, M. Sanz, J.A. Cobos, P. Alou, O. Garcia and J. Uceda, "Design considerations of multi-layer piezoelectric transformers," APEC '01, March 2001, pp. 1258 - 1263.

[5] Junhui Hu, "Temperature field of the piezoelectric transformer operating in longitudinal vibration mode," Ultrasonics Symposium, 2002, Oct. 2002, pp. 1003 – 1006.

[6] S. Bronstein and S. Ben-Yaakov, "Design considerations for achieving ZVS in a half bridge inverter that drives a piezoelectric transformer with no series inductor," PESC '02, June 2002, pp. 585 – 590.

[7] D. Vasic, F. Costa and E. Sarraute, "A new method to design piezoelectric transformer used in MOSFET and IGBT gate drive circuits," PESC '03, June 2003, pp. 307 – 312.

[8] T Zaitsu, T Shigehisa, T Inoue, M Shoyama, T Ninomiya, "Piezoelectric transformer converter with frequency control," INTELEC '95, Oct. 1995, pp. 175 – 180.

[9] T. Zaitsu, T. Shigehisa, M. Shoyama and T. Ninomiya, "Piezoelectric Transformer Converter with PWM Control," APEC '96, March 1996, pp. 279-283.

[10] S. Hamamura and D. Kurose, "New control method of piezoelectric transformer converter by PWM and PFM for wide range of input voltage," CIEP '00, Oct. 2000, pp. 3 – 8.

[11] Sungjin Choi, Taeil Kim and B.H. Cho, "Design of half-bridge piezo-transformer converters in the AC adapter applications," APEC '05, March 2005, pp. 244 – 248.

[12] T. Yamane, S. Hamamura, T. Zaitsu, T. Minomiya, M. Shoyama and Y. Fuda, "Efficiency improvement of piezoelectric-transformer DC-DC converter," PESC '98, May 1998, pp. 1255 – 1261.